CLAIMS

What is claimed is:

1. A semiconductor memory device comprising:

an internal voltage generator receiving a power supply voltage from an exterior for generating an internal voltage to be supplied to an internal circuit; and

an entry circuit for inactivating said internal voltage generator in response to a control signal received from the exterior and entering the device into a low power consumption mode.

2. A semiconductor memory device according to Claim 1, further comprising a word line connected with memory cells, and wherein

said internal voltage generator includes a booster for generating a boost voltage to be supplied to said word line.

3. A semiconductor memory device according to Claim 1, wherein said internal voltage generator includes a substrate voltage generator for generating a substrate voltage to be supplied to a substrate.

4. A semiconductor memory device according to Claim 1, further comprising a memory core having a plurality of memory cells, and wherein

said internal voltage generator includes an internal supply voltage generator for generating an internal supply voltage to be supplied to said memory core lower than said supply voltage.

5. A semiconductor memory device according to Claim 1, further comprising a memory core including memory cells and a bit line connected with memory cells, and wherein

said internal voltage generator includes a precharging voltage generator for generating a precharging voltage to be supplied to said bit line.

6. A semiconductor memory device according to Claim 1, further comprising an external

voltage supplying circuit for supplying said power supply voltage as said internal voltage to said internal circuit during said low power consumption mode.

7. A semiconductor memory device according to Claim 1, wherein said entry circuit receives a reset signal for inactivating said internal circuit from the exterior and enters the device into said low power consumption mode.

8. A semiconductor memory device according to Claim 1, wherein said entry circuit receives a plurality of control signals from the exterior and enters the device into said low power consumption mode when the levels of the control signals indicate a low power consumption command.

9. A semiconductor memory device according to Claim 8, wherein said entry circuit receives from the exterior a reset signal for inactivating said internal circuit and a chip enable signal for activating a part of said internal circuit to be operated in a read/write operation and enters the device into said low power consumption mode when the levels of the reset signal and the chip enable signal indicate said low power consumption command.

10. A semiconductor memory device according to Claim 9, wherein said entry circuit enters the device into said low power consumption mode when said reset signal is inactivated during a predetermined period and then said chip enable signal is activated during a predetermined period.

11. A semiconductor memory device according to Claim 8, wherein said entry circuit receives said plurality of control signals during said low power consumption mode and exits the device from the low power consumption mode when the levels of said control signals indicate exit of the low power consumption mode.

12. A semiconductor memory device according to Claim 1, wherein:

said control signal includes a low power consumption mode signal; and

said entry circuit receives the predetermined level or the transition edge of said low power consumption mode signal and enters the device into said low power consumption mode.

13. A semiconductor memory device comprising:

an internal voltage generator receiving a power supply voltage from an exterior for generating an internal voltage to be supplied to an internal circuit; and

an entry circuit for inactivating said internal voltage generator in response to a control signal received from the exterior and entering the device into a low power consumption mode, and

wherein said entry circuit receives said control signal during said low power consumption mode and exits the device from said low power consumption mode when the state of said control signal indicates exit of said low power consumption mode.

14. A semiconductor memory device according to Claim 13,

wherein a reset signal for initializing an internal circuit is activated during a period where said internal voltage is lower than a predetermined voltage after the device is exited from said lower power consumption mode.

15. A semiconductor memory device according to Claim 14,

wherein said predetermined voltage is a reference voltage which is generated by stepping down said power supply voltage.

16. A semiconductor memory device according to Claim 13,

wherein a reset signal for initializing an internal circuit is activated during a period where a boost voltage internally generated is lower than a predetermined voltage after the device is exited from said lower power consumption mode.

17. A semiconductor memory device according to Claim 16,

wherein said predetermined voltage is said power supply voltage.

18. A semiconductor memory device according to Claim 16,

wherein said predetermined voltage is said reference voltage which is generated by stepping down said power supply voltage.

19. A semiconductor memory device according to Claim 13,

wherein a reset signal for initializing an internal circuit is activated during a period wherein at least one of said internal voltage and a boost voltage internally generated is/are lower than respective predetermined voltages after the device is exited from said lower power consumption mode.

20. A semiconductor memory device according to Claim 13, further comprising a timer for measuring a predetermined length of time after the device is exited from said lower power consumption mode, and wherein

a reset signal for initializing an internal circuit is activated during said predetermined length of time.

21. A semiconductor memory device according to Claim 20,

wherein said timer includes a CR time constant circuit; and

said predetermined length of time is measured based on the propagation delay time of a signal propagated to said CR time constant circuit.

22. A semiconductor memory device according to Claim 20,

wherein said timer includes a counter which operates during a normal operation; and

said predetermined length of time is measured based on a count value of said counter.

23. A semiconductor memory device according to Claim 22,

wherein said counter is a refresh counter which indicates refresh address of memory cells.

24. A semiconductor memory device comprising:

a self-refresh control circuit for automatically refreshing memory cells at a predetermined cycle; and

an internal voltage generator for generating an internal voltage to be supplied to a predetermined internal circuit, upon receipt of a power supply voltage from an exterior, and wherein

said self-refresh control circuit is inactivated, and supply capacity of said internal voltage in said internal voltage generator is lowered when a control signal is received from the exterior, thereby entering the device into a low power consumption mode.

25. A semiconductor memory device according to Claim 24,

wherein said internal voltage generator includes a plurality of units for generating said internal voltage; and

a part of said units suspend(s) during said low power consumption mode.

26. A semiconductor memory device comprising:

a stabilized capacitor connected with a power supply line for storing a portion of electric charge to be supplied to said power supply line; and

an internal circuit connected with said power supply line, and wherein

a connection between said power supply line and said stabilized capacitor is maintained and said power supply line and said internal circuit is disconnected when a control signal is received from the exterior, thereby entering the device into a low power consumption mode.

27. A semiconductor memory device according to Claim 26,

further comprising:

an internal voltage generator for generating an internal voltage upon receipt of a

power supply voltage from the exterior, and wherein

said internal voltage is supplied to said internal circuit through said power supply line.

28. A semiconductor memory device comprising:

an internal voltage generator for generating an internal voltage to be supplied to a predetermined internal circuit upon receipt of a power supply voltage from an exterior; and

an internal voltage detector for detecting a level of said internal voltage and controlling said internal voltage generator according to a detection result, and wherein

detection capability of said internal voltage detector is lowered when a control signal is received from an exterior, thereby entering the device into a low power consumption mode.

29. A semiconductor memory device according to Claim 28,

wherein said internal voltage generator includes a plurality of units for detecting a level of said internal voltage; and

a part of said units suspend(s) during said low power consumption mode.

30. A semiconductor memory device comprising:

an internal voltage generator for generating an internal voltage to be supplied to a predetermined internal circuit upon receipt of a power supply voltage from an exterior, and

an internal voltage detector for detecting a level of said internal voltage and controlling said internal voltage generator according to a detection result, and wherein

when a control signal is received from the exterior, the absolute value of said internal voltage generated by said internal voltage generator is reduced by lowering the detection level of said internal voltage in said internal voltage detector, thereby entering the device into a low power consumption mode.

31. A semiconductor memory device according to Claim 30,

further comprising a reference voltage generator for generating a reference voltage, and wherein

said internal voltage detector detects the level of said internal voltage by comparing said internal voltage with said reference voltage; and

when a control signal is received from the exterior, the detection level of said internal voltage in said internal voltage detector is lowered by decreasing the level of said reference voltage generated by said reference voltage generator.

32. A semiconductor memory device comprising:

a self-refresh control circuit for automatically refreshing memory cells at a predetermined cycle, and wherein

when a control signal is received from an exterior, said self-refresh control circuit is inactivated, thereby entering the device into a low power consumption mode.

33. A semiconductor memory device according to Claim 32,

wherein said self-refresh control circuit includes a timer for determining a length of refresh cycle; and

said timer suspends during said low power consumption mode.

34. A method of controlling a semiconductor memory device, comprising an internal voltage generator receiving a power supply voltage from an exterior for generating an internal voltage to be supplied to an internal circuit, said method comprising the steps of:

inactivating said internal voltage generator in response to a control signal received from the exterior; and

entering the device into a low power consumption mode.

35. A method of controlling a semiconductor memory device according to Claim 34, wherein:

said control signal comprises a plurality of control signals; and

the device enters into said low power consumption mode when a logical combination of said control signals indicate a low power consumption command.

36. A method of controlling a semiconductor memory device according to Claim 35, wherein:

the device enters into said low power consumption mode when a reset signal for inactivating said internal circuit is inactivated and then a chip enable signal for activating a part of said internal circuit to be operated in a read/write operation is activated, and wherein

said reset signal is inactivated when the power supply is switched on.

37. A method of controlling a semiconductor memory device, comprising an internal voltage generator receiving a power supply voltage from an exterior for generating an internal voltage to be supplied to an internal circuit, said method comprising the steps of:

inactivating said internal voltage generator in response to a control signal received from the exterior and entering the device into a low power consumption mode; and

receiving said control signal during said low power consumption mode and exiting the device from said low power consumption mode when the state of said control signal indicates exit of said low power consumption mode.

38. A method of controlling a semiconductor memory device according to Claim 37,

wherein a reset signal for initializing an internal circuit is activated during a period where said internal voltage is lower than a predetermined voltage after the device is exited from said lower power consumption mode.

39. A method of controlling a semiconductor memory device comprising a self-refresh control circuit for automatically refreshing memory cells at a predetermined cycle; and

an internal voltage generator for generating an internal voltage to be supplied to a

predetermined internal circuit upon receipt of a power supply voltage from an exterior, further comprising the steps of:

inactivating said self-refresh control circuit and lowering supply capability of said internal voltage in said internal voltage generator when a control signal is received from the exterior; and

entering the device into a low power consumption mode.

40. A method of controlling a semiconductor memory device comprising a stabilized capacitor connected with a power supply line for storing a portion of electric charge to be supplied to said power supply line; and

an internal circuit connected with said power supply line, further comprising the steps of:

maintaining a connection between said power supply line and said stabilized capacitor and disconnecting said power supply line and said internal circuit when a control signal is received from the exterior; and

entering the device into a low power consumption mode.

41. A method of controlling a semiconductor memory device comprising an internal voltage generator for generating an internal voltage to be supplied to a predetermined internal circuit upon receipt of a power supply voltage from an exterior; and

an internal voltage detector for detecting a level of said internal voltage and controlling said internal voltage generator according to a detection result, further comprising the steps of:

lowering the detection capability of said internal voltage detector when a control signal is received from an exterior; and

entering the device into a low power consumption mode.

42. A method of controlling a semiconductor memory device comprising an internal voltage generator for generating an internal voltage to be supplied to a predetermined internal circuit upon receipt of a power supply voltage from an exterior; and

an internal voltage detector for detecting a level of said internal voltage and controlling said internal voltage generator according to a detection result, further comprising the steps of:

reducing the absolute value of said internal voltage generated by said internal voltage generator by lowering the detection level of said internal voltage in said internal voltage detector when a control signal is received from the exterior; and

entering the device into a low power consumption mode.

43. A method of controlling a semiconductor memory device comprising a self-refresh control circuit for automatically refreshing memory cells at a predetermined cycle, further comprising the steps of:

inactivating said self-refresh control circuit when a control signal is received from an exterior; and

entering the device into a low power consumption mode.